

PATENT

REMARKS

This paper is responsive to the Non-Final Office Action dated July 27, 2005. Claims 1-23 were examined. Claims 1-23 stand rejected under 35 U.S.C. 102(e) as being unpatentable by U.S. Patent No. 6,687,888 to Chen.

Claim Rejections - 35 U.S.C. § 102

Claims 1-23 stand rejected under 35 U.S.C. 102(e) as being unpatentable by Chen (U.S. Patent 6,687,888). Claim 1 is amended to clarify the invention. Applicants believe that Chen, alone or in combination with other references of record, fails to teach or suggest

selecting a subset of low threshold voltage variants of gate instances for substitution with respective standard threshold voltage variants thereof based on at least a maximum of the first set of path cycle times and a maximum of the second set of path cycle times for a corresponding low threshold voltage variant.

Chen teaches that

[e]ach state in the population is then scored 408 for timing and for power dissipation. Delay for each path from clock to clock in the partition is calculated, and each delay total is compared to timing constraints. If any path exceeds timing constraints, the score for the individual is negatively affected...Individual states from the population are selected 410 for survival based on their score. Those states having the best score are guaranteed survival; those having lower scores are granted a lower, but finite probability of survival.

Col. 9, lines 52-65. Nowhere does Chen teach or suggest selecting a subset of low threshold voltage variants of gate instances for substitution with respective standard threshold voltage variants thereof based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant consistent with the limitations of amended claim 1. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

PATENT

Claim 15 is amended to clarify the invention. Applicants believe that Chen, alone or in combination with other references of record, fails to teach or suggest

a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant.

Chen teaches that

[e]ach state in the population is then scored 408 for timing and for power dissipation. Delay for each path from clock to clock in the partition is calculated, and each delay total is compared to timing constraints. If any path exceeds timing constraints, the score for the individual is negatively affected...Individual states from the population are selected 410 for survival based on their score. Those states having the best score are guaranteed survival; those having lower scores are granted a lower, but finite probability of survival.

Col. 9, lines 52-65. Nowhere does Chen teach or suggest a subset of the gate instances that are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant consistent with the limitations of amended claim 15. Accordingly, Applicants respectfully request that the rejection of claim 15 and all claims dependent thereon, be withdrawn.

Claim 18 is amended to clarify the invention. Applicants believe that Chen, alone or in combination with other references of record, fails to teach or suggest

a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant.

PATENT

Chen teaches that

[e]ach state in the population is then scored 408 for timing and for power dissipation. Delay for each path from clock to clock in the partition is calculated, and each delay total is compared to timing constraints. If any path exceeds timing constraints, the score for the individual is negatively affected...Individual states from the population are selected 410 for survival based on their score. Those states having the best score are guaranteed survival; those having lower scores are granted a lower, but finite probability of survival.

Col. 9, lines 52-65. Nowhere does Chen teach or suggest a subset of the gate instances that are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant consistent with the limitations of amended claim 18. Accordingly, Applicants respectfully request that the rejection of claim 18 and all claims dependent thereon, be withdrawn.

Claim 20 is amended to clarify the invention. Applicants believe that Chen, alone or in combination with other references of record, fails to teach or suggest that

a subset of the gate instances are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant.

Chen teaches that

[e]ach state in the population is then scored 408 for timing and for power dissipation. Delay for each path from clock to clock in the partition is calculated, and each delay total is compared to timing constraints. If any path exceeds timing constraints, the score for the individual is negatively affected...Individual states from the population are selected 410 for survival based on their score. Those states having the best score are guaranteed survival; those having lower scores are granted a lower, but finite probability of survival.

Col. 9, lines 52-65. Nowhere does Chen teach or suggest a subset of gate instances that are standard threshold voltage variants substituted in the semiconductor integrated circuit based on at

PATENT

least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant consistent with the limitations of amended claim 20. Accordingly, Applicants respectfully request that the rejection of claim 20 and all claims dependent thereon, be withdrawn.

Claim 23 is amended to clarify the invention. Applicants believe that Chen, alone or in combination with other references of record, fails to teach or suggest that

at least one of the low threshold voltage gate instance representations is selected based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant.

Chen teaches that

[e]ach state in the population is then scored 408 for timing and for power dissipation. Delay for each path from clock to clock in the partition is calculated, and each delay total is compared to timing constraints. If any path exceeds timing constraints, the score for the individual is negatively affected...Individual states from the population are selected 410 for survival based on their score. Those states having the best score are guaranteed survival; those having lower scores are granted a lower, but finite probability of survival.

Col. 9, lines 52-65. Nowhere does Chen teach or suggest a subset of gate instances that are standard threshold voltage variants is selected based on at least a maximum of a first set of path cycle times and a maximum of a second set of path cycle times for a corresponding low threshold voltage variant consistent with the limitations of amended claim 23. Accordingly, Applicants respectfully request that the rejection of claim 23 and all claims dependent thereon, be withdrawn.

Additional Remarks

Claims 2 and 5-10 are canceled, consistent with amendments to claim 1. Claims 3, 4, and 11 are amended consistent with amendments to claim 1 and to clarify the invention.

PATENT

Claims 3, 4, and 11 are amended consistent with amendments to claim 1 and to clarify the invention.

Claims 16 and 17 are amended consistent with amendments to claim 15 and to clarify the invention.

Claim 19 is amended consistent with amendments to claim 18 and to clarify the invention.

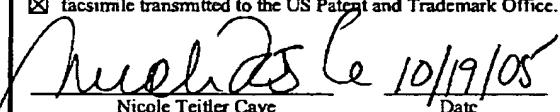
Claim 21 is canceled consistent with amendments to claim 20.

Claim 22 is amended consistent with amendments to claim 22 and to clarify the invention.

New claims 24-31 are added. Applicants believe that new claims 24-31 depend from allowable base claims and are allowable for at least this reason.

Summary

All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,



Nicole Teitler Cave, Reg. No. 54,021  
Attorney for Applicant(s)  
(512) 338-6315 (direct)  
(512) 338-6300 (main)  
(512) 338-6301 (fax)